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Protecting People and the Environment

DAC Inspection

Status

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Overview

- DAC Inspection Procedures
- STP pre-COL DAC Inspection (Pt 2)
- Resolution and Closure Process
- ESBWR DI&C DAC

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DAC Inspection Procedures

- **DI&C DAC IP (65001.xx) developed in stages per ACRS commitment; IP w/ App. 1 thru 3 completed 9/30 (ML102650556)**
- **Draft DI&C DAC IP (w/ all appendices) due 12/2010**
- **Piping DAC IP drafted; target date for issuance is 12/2010**
- **HFE DAC IP(s) to be contractor- developed; drafts expected 6/2011**

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STP pre-COL DAC Inspection - Part 2

- **Part 1 Recap:**
  - **STP "project" level planning/process docs**
  - **ABWR DCD T1, 3.4.7 thru 3.4.10**
  - **IR 2010-001 issued in August**

- **Part 2 Objective:**
  - **Toshiba FPGA "platform" level Planning Phase activities**

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Inspection Scope (Lesson Learned)

- **DCD T1, 3.4.11 Acceptance Criteria:**

  "S/W development has been completed as defined in SMP, CMP and V&VP"

- **Safety-related software development process (Planning Phase) is outlined in 3.4.8.d**
  - **"platform" level Plan implementation**
  - **equipment design requirements**
  - **safety analysis of design requirements**
  - **issue(s) management (nonconformances)**

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Part 2 Inspection

- Toshiba NEF and FPGA Mfg. in Isogo and Fuchu, Japan
- Planning Phase scheduled to complete in 2010; inspection ~Feb 2011
- Inspection complement: 2 RII inspectors w/ 2 NRO technical staff
- Draft DI&C DAC IP 65001.xx (w/ App. 1 & 2) informed by IP35007
- Inspection concurrent w/ VQA inspection at Toshiba

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IP 65001.xx (Draft)

- Six appendices (DI&C software life cycle correlation)
- Part 2 inspection will use Appendices 1 (Planning) and 2 (Requirements)
- Appendix 1 used in Part 1 inspection
- Appendix 2:
  - sample of requirements (SRS) attributes
  - thread audits (sample of critical reqmts)
  - documentation assessment
  - safety analysis assessment

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2011 DAC Inspection (projected)

- **STP – Toshiba FPGA Planning Phase (Feb 2011**
- **STP – Westinghouse (Common Q platform) Planning Phase (mid 2011)**
- **STP – Toshiba FPGA Design Definition Phase (late 2011)**

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Process Refinement

- Modify NEI 08-01 Section 8.3 (DAC) to be consistent with agency approach
- Revise RG 1.215 accordingly
- Fully integrate with ITAAC closure process
- Make process applicable to all design centers (generic)

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ESBWR DI&C DAC

- GEH repackaged DI&C DAC in Rev 8 of DCD
- Inventory includes ~400 discrete DAC

- In conjunction w/ ITAAC prioritization, staff developing a plan for managing the inspection (verification) effort for these DAC

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Path Forward

- Plan for STP DAC inspections
- Complete DI&C DAC IP
- Continue work on HFE DAC IP and Piping DAC IP issuance
- Address ESBWR DI&C DAC inventory
- Work w/ stakeholders to revise NEI 08-01 and RG 1.215